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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,985	03/08/2002	Steven H. Voldman	BUR920020014	2597

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EXAMINER	
NADAV, ORI	
ART UNIT	**PAPER NUMBER**
2811	

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10/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/683,985	VOLDMAN, STEVEN H.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-29,31-42 and 44-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-29,31-42 and 44-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 35-38 should be withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected embodiment, there being no allowable generic or linking claim. Applicant states, in the response filed on 8/9/2007, that claim 33 reads on the embodiment of figure 3. The restriction requirements filed on 10/1/2003 required applicant to elect between the embodiments of figures 1-3, 4-5 and 6-7. Therefore, it appears that applicant elected the embodiment of figures 1-3 for examination. As a result, claims 35-38, which read on the embodiment of figures 4-5, should be withdrawn from consideration.

Claim Objections

Claims 26-29, 31-42 and 44-47 are objected to because of the following informalities: The phrase "a depth less than said cathode", as recited in claim 26, should read "a depth less than that of said cathode". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-29, 31-32, 39-42 and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu (6,437,383) in view of Hargrove et al. (5,731,941). Regarding claims 26 and 29, Xu teaches in figures 7-10 and related text a method of forming a diode comprising the steps of:

providing an original substrate 120 not doped with anode and cathode regions and forming an anode 160 of a first conductivity type and a cathode 150 of a second conductivity type disposed below said anode on said original substrate without removing any portion of said original substrate and without replacing with another substrate material, wherein

at least one of said cathode and anode comprise a plurality of vertically abutting diffusion regions 140, 150, and

forming a plurality of isolation regions 130 in said original substrate, said cathode and anode being disposed between adjacent ones of said plurality of isolation regions, said plurality of isolation regions extending deeper into said original substrate than said cathode and said anode, wherein

said step of forming said cathode comprises forming a first doped region 150 of a second conductivity type abutting said anode 160, and forming a second doped region140 of said second conductivity type abutting and disposed below said first doped region and contacting said original substrate, said first and second doped regions having different dopant concentrations.

Xu does not teach forming a plurality of isolation structures in said original substrate, wherein each of said plurality of isolation structures disposed between at least a portion

of said anode and respective said adjacent ones of said plurality of isolation regions, said plurality of isolation structures extend to a depth less than said cathode.

Hargrove et al. teach in figure 4 and related text a plurality of isolation structures STI in an original substrate, wherein each of said plurality of isolation structures STI disposed between at least a portion of an anode P+ and respective adjacent ones of plurality of isolation regions 34, said plurality of isolation structures STI extend to a depth less than said cathode (N well).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of isolation structures in said original substrate, wherein each of said plurality of isolation structures disposed between at least a portion of said anode and respective said adjacent ones of said plurality of isolation regions, said plurality of isolation structures extend to a depth less than said cathode, in Xu's device, in order to provide better protection to the diode.

Note that the broad recitation of the claims does not require that each of the plurality of isolation structures to be in direct contact with a portion of said anode and with respective said adjacent ones of said plurality of isolation regions.

Regarding claim 27, Xu teaches in figures 7-10 and related text a plurality of insulation-filled trenches having sidewalls that are substantially vertical.

Regarding claim 28, Xu teaches substantially the entire claimed structure, as applied to claim 26 above, except isolation regions having tapered sidewalls.

Hargrove et al. teach in figure 4 and related text isolation regions 34 having tapered sidewalls.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use isolation regions having tapered sidewalls in Xu's device in order to improve the isolation of the device and in order to adjust the device characteristics.

Regarding claim 30, Xu teaches in figures 7-10 and related text forming a second pair of isolation structures 132 between said adjacent isolation regions and said anode.

Regarding claims 39-41, Xu teaches in figures 7-10 and related text said cathode being in electrical contact with said substrate and is disposed entirely below said anode, wherein a junction formed between said anode and said cathode is bounded by said adjacent ones of said plurality of isolation regions.

Regarding claims 31-32, Xu teaches in figures 7-10 and related text substantially the entire claimed structure, as applied to claim 26 above, except explicitly stating that isolation regions 130 are formed by a process comprising the steps of etching said substrate to form trenches and depositing at least one insulator, removing portions of said insulator outside of said trenches, and depositing a fill material.

Xu teaches in figures 7-10 and related text isolation regions 132 are formed by a process comprising the steps of etching said substrate to form trenches and depositing

at least one insulator, removing portions of said insulator outside of said trenches, and depositing a fill material.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form isolation regions 130 by a process comprising the steps of etching said substrate to form trenches and depositing at least one insulator, removing portions of said insulator outside of said trenches, and depositing a fill material in Xu's device, in order to simplify the processing steps of making the device by using conventional processing steps.

Regarding claim 42, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a single crystal substrate in Xu's device in order to improve the characteristics of the device.

Regarding claims 44 and 46-47, Xu teaches in figure 7 and related text a step of forming said anode/cathode and a step of forming a doped region for a transistor in another region of said original substrate (adjacent regions) occur substantially simultaneously, and epitaxially growing a layer on said original substrate to substantially simultaneously form said cathode and said doped region for said transistor.

Regarding claim 45, Xu teaches in figure 7 and related text epitaxially growing a layer on said original substrate, but does not teach substantially simultaneously form said

anode and a base region for said transistor. Hargrove et al. teach in figure 4 and related text forming a base region (N well) for a transistor.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to substantially simultaneously form said anode and a base region for said transistor in Xu's device, in order to simplify the processing steps of making the device when using the device in an application which requires a circuit comprising PNP transistor.

Claims 33, 35 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu and Hargrove et al., as applied to claim 26 above, and further in view of Chen et al. (6,242,763).
Regarding claim 33, Xu and Hargrove et al. teach substantially the entire claimed structure, as applied to claims 26 and 29 above, except a third doped region 211 disposed between a first doped region and a second doped region.
Chen et al. teach in figure 3 and related text forming a third doped region 211 disposed between a first doped region and a second doped region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a third doped region between said first doped region and said second doped region in prior art's device in order to improve the characteristics of the device.

Regarding claim 35, Chen et al. teach in figure 3 and related text an anode comprises

a first doped region 206 and a second doped region 210 on a surface of a substrate, wherein said second doped region having a higher concentration of dopant than said first doped region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an anode in prior art's device having a first doped region abutting said cathode; and a second doped region on a surface of said substrate, wherein said second doped region having a higher concentration of dopant than said first doped region, in order to improve the characteristics of the device.

Regarding claims 37-38, Xu teaches in figures 7-10 and related text forming a plurality of diffusion regions 140 of said second conductivity type on a surface of said substrate, and forming a plurality of second isolation regions 132 that separate said plurality of diffusion regions from said cathode.

Claims 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xu, Hargrove et al. and Chen et al., as applied to claims 33 and 35 above, and further in view of Robinson et al. (5,268,316).

Xu, Hargrove et al. and Chen et al. teach substantially the entire claimed structure, as applied to claims 26, 29, 33 and 35 above, except a third doped region comprises a retrograde-doped region. Robinson et al. teach a third doped region comprises a retrograde-doped region (column 3, lines 36-47). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third

doped region comprises a retrograde-doped region in prior art's device in order to provide low-reverse leakage, a relatively low voltage turn-on, and low series resistance for the current path from the junction to the diode contact.

Response to Arguments

Applicant's arguments with respect to claims 26-29, 31-42 and 44-47 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

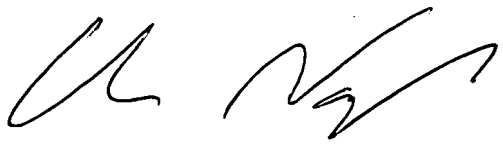
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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9/28/07

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